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Thapar University Patiala, ECED

MTech (VLSI & CAD)
II Semester, MST , March 2009
Time : 2 Hours, MM: 35

VL010: Low Power CMOS Circuit Design
Course Coordinator: Arun Kr. Chatterjee

NOTE: Attempt all problems. Assume any missing data/ information.

1. What do you understand by power dissipation in CMOS circuits? Explain its types. Show that for a CMOS inverter $P_{sc} = \beta/12\ (V_{tp}- V_{tn})^3 \tau / T$ where the symbols have their usual meaning. (6)

2. What are the various effects which influence Threshold Voltage of a MOS, explain. (6)

3. Show that within the weak inversion saturation region drain current , I_D, is of the form of (6)

$$I_1 \exp (V_{GS}/V_1)$$

With the help of MOS characteristic and deduce the values for I_1 and V_1.

4. What is back Gate effect. Discuss it's effect on MOS operation. (5)

5. Explain the need and basic principles of low power design. (5)

6. A 28 bit off chip bus operating at 5V and 66 MHz clock rate is driving a capacitance of 25 pF/bit. Each bit is estimated to have a toggling probability of 0.35 at each clock cycle. What is the power dissipation in operating the bus. (3)

7. Explain temperature variation effects on mobility of charge carriers and Threshold voltage of MOSFET. (4)