Code No: R05220504 **Set No. 1**

II B.Tech II Semester Regular Examinations, Apr/May 2008
MICROPROCESSORS AND INTERFACING
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain various interrupts of 8085 Microprocessor and their functionality?
   (b) Explain the [8+8]
      i. SID
      ii. SOD
      iii. S0, S1, S2
      iv. INTA pins of 8085 Microprocessor.

2. (a) Explain in detail the coding template for ADD instruction of 8086.
   (b) It is necessary to declare a program as a public procedure to be accessible by other programs? Give the sequence of assembly language statements? An external program called "fact" is to used in this program. Show the required statements? [8+8]

3. Write a recursive routine to evaluate the following polynomial

   Y = A_0+A_1X_1+A_2X_2+A_3X_3+....+ANXN. The coefficients A0, A1, A2....AN are to be successive words in memory and all parameter addresses are to be passed via the stack. [16]

4. (a) With a neat sketch explain 8237 DMA controller and its operation?
   (b) With the help of basic cell explain SRAM and DRAM? [8+8]

5. (a) Interface the stepper motor with 8255 and write an ALP to rotate the stepper motor continuously in clockwise direction.
   (b) Write an assembly language program to rotate a 200 teeth, 4 phase stepper motor as specified below: Ten rotations clockwise and eight rotations anti-clockwise. [8+8]

6. (a) What is the interrupt vector table? Draw and explain the interrupt vector table for 8086.
   (b) Describe the response of 8086 to the interrupt coming on INTR pin. [8+8]

7. (a) What is a Status word of 8251A? Explain how 8086 processor will read the status word from 8251.
   (b) Write the sequence of instructions required to initialize 8251 at address A0H and A1H for the configuration given below: [8+8]

i. Character length - 8 bits.
ii. No parity
iii. Stop bits - 1 1/2
iv. Baud rate - 16X
v. DTR and RTS asserted
vi. Error flag reset.

8. (a) How does 8051 differentiate between the external and internal program memory?
   (b) Explain the alternate functions of Port-0, Port-2 and Port-3. [8+8]

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1. (a) Explain the flag register of 8086.
   (b) Explain the concept of memory segmentation.
   (c) Explain, when Queue is failing to speed up the execution. [6+6+4]
2. (a) How does near RET instruction function ?
   (b) Write a near procedure that cubes the contents of the CX register.This procedure may not affect any register except CX. [8+8]
3. Write an algorithm and assembly program to sort the numbers in an array in descending order using bubble sort method. [16]
4. (a) With a neat sketch explain 8237 DMA controller and its operation?
   (b) With the help of basic cell explain SRAM and DRAM? [8+8]
5. Explain the following terms in relation to 8279:
   (a) Two key lockout
   (b) N-key rollover
   (c) Right entry
   (d) Left entry
   (e) FIFO
   (f) Display RAM
   (g) Blanking
   (h) Key de-bounce. [2×8]
6. (a) List out the advantages of using 8259?
   (b) Describe the conditions that cause the 8086 to perform each of the following types of interrupts: Type-0, Type-1, Type-2 and Type-4. [8+8]
7. (a) Explain the line driver and the line receiver circuits of serial communication.
   (b) What do you mean by I/O mapped I/O? Draw the interfacing of 8251 with 8086 in I/O mapped I/O mode. [8+8]
8. (a) Discuss the advantages of microcontroller based system over microprocessor based systems.

(b) Describe the following registers of 8051: [8+8]

i. A
ii. B
iii. SP
iv. DPTR.

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Code No: R05220504 **Set No. 3**

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1. (a) Draw the internal architecture of 8085? Explain about each block in it.
   (b) Explain the function of OPCODE prefetch FIFO Buffer in 8086? [10+6]

2. (a) Explain the following instructions and their use?
      i. LODSB
      ii. CMPSW
      iii. XLAT.
   (b) Give the instruction format of IN and OUT instructions and explain? [9+7]

3. (a) Write a program to sort an array in descending order.
   (b) Give the instruction sequence that compares the first 20 bytes beginning at STRG 1with the first ten bytes beginning at STRG 2 and branches to MATCH if they are equal, otherwise continues in sequence? [8+8]

4. (a) What are the contents of the data bus and the status of A_0 and $\overline{BHE}$ when the following instructions are executed in 8086?
      i. CPU writes a byte 11 H at memory location 1000H : 0002 H.
      ii. CPU writes a word 2211 H at memory location 1000H : 0003 H.
   (b) Write the functions of the following pins of 8086.
      i. MN/ $\overline{MX}$
      ii. $\overline{DEN}$
      iii. ALE
      iv. Ready.
   (c) Draw a block diagram to interface two 16K X 8 SRAM (62128) to the 16-bit data bus of 8086 based system. Design the address decoder for the address range from 00000H - 07FFFFH for both the SRAMs. [5+5+6]

5. (a) Draw the interfacing scheme of 8255 and 8086 in memory mapped I/O mode.
   (b) An 8255 is used with port-A input in mode-1, Port-B as output in mode-1 and with Port-C used for handshaking for Port-A and Port-B. Assume the address of Port-A is 80H.
      i. Determine the control word and write the instruction sequence to program the 8255 for this mode of operation.

ii. Draw the scheme of connections required. [8+8]

6. (a) Discuss the sequence of operations performed in the interrupt acknowledge cycle.
   (b) What is the difference between RET and IRET? Discuss the result, if RET instruction is placed at the end of the interrupt service routine.
   (c) What is the vector address of type-50H interrupt? [6+6+4]

7. Design the hardware interface circuit for interfacing 8251 with 8086. Set the 8251 in asynchronous mode as a transmitter and receiver with even parity enabled, 2 stop bits, 8-bit character length, frequency 160 KHz and baud rate 10K:
   (a) Write an ALP to transmit 100 bytes of data string starting at location 2000:5000H.
   (b) Write an ALP to receive 100 bytes of data string and store it at 3000:4000H. [8+8]

8. (a) Explain various operation modes of Timer-1 and Timer-0.
   (b) Describe the Timer control (TCON) and Timer mode control (TMOD) registers. [16]

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Code No: R05220504 **Set No. 4**

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1. (a) Explain the functions of different registers in 8086. Also discuss the flag register contents.
   (b) How procedure CALL and RET take place in 8086. Explain conditional and unconditional CALL and RET instructions in 8086 instruction set. [6+10]

2. (a) Write a program to move a block of memory with out over lapping.
   (b) Discuss the following instructions. [8+8]
      i. ADC
      ii. AAS
      iii. IMUL
      iv. CBW.

3. (a) Write an assembly language program that will examine an ASCII string of 100 characters and replace each decimal digit by a %. The character string starts at STRG.
   (b) Explain the prefix instruction format of 8086 processor? Discuss how these instructions are useful in string manipulation? [8+8]

4. (a) With a neat sketch explain 8237 DMA controller and its operation?
   (b) With the help of basic cell explain SRAM and DRAM? [8+8]

5. Write the necessary instruction sequence to initialize 8255 with address 0200H to 0203H for the following combinations:
   (a) Port-A as input port in mode-1 and Port-B as input port in mode-1 with interrupt driven I/O.
   (b) Port-A in mode-2 and Port-B as input port in mode-1 with interrupt driven I/O.
   (c) Port-A as output port in mode-0 and Port-C upper half as input port in mode-0, and Port-B as output port in mode-1 with interrupt driven I/O.
   (d) Port-A as output port in mode-1 with active interrupt, Port-B as output port in mode-0 and Port-C lower half as input port in mode-0. [4 × 4]

6. What is an interrupt? Explain, how the 8086 processor recognizes the interrupt? Draw the timing diagram, assuming that INTR is active. Explain interrupt acknowledge cycle with its associated timing diagram. [16]

7. (a) Draw and explain the null modem interfacing.
   (b) What is Memory mapped I/O? Draw the interfacing of 8251 with 8086 in memory mapped I/O mode. [8+8]

8. Give the complete block schematic of an 8051 based system having following specifications:
   (a) 64 KB program memory
   (b) 64 KB data memory
   (c) Make use of 16 K x 8-bit memory chips and 74LS138 decoders.
   (d) Indicate clearly the address selected for the memory chips. [4×4]

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